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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/691,115	10/19/2000	Yukihiro Nomura	P108066-00014	5084

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	5

DATE MAILED: 02/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/691,115	Applicant(s) NOMURA ET AL.	
	Examiner James C Kerveros	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims1-39 are rejected under 35 U.S.C. 102(e) as being anticipated by Park (US 6108252).

Regarding independent Claims 1, 26 and 38, Park discloses a self-test circuit (BIST 105) that detects defects of a memory device, incorporated in the memory device having a memory control circuit that controls write and read operations with respect to a memory core (101) including two banks, in response to a command (BISTON), as shown in (FIGS. 1 and 2) comprising:

A test operation command generating circuit (BIST controller 211), which is part of the self-test circuit (BIST 105), generates a test operation command control signal CON for the memory control circuit that designates the writing or reading of the input data (DRIN) and the output data (DROUT) to / from the memory core (101), using the write enable (WEB0 and WEB1) command, in

response to external clock TCLKT and BIST mode BISTON command, during the self-test activated condition (BIST mode of operation).

A test address generating circuit (203), that during the BIST mode of operation, generates a test address (RADD and CADD) provided for the memory core (101).

A test data generating circuit (data generator 213), that during the BIST mode of operation, generates test data (DRIN) provided for the memory core (101).

A test output circuit comparator (205) located in the BIST 105, which compares the signal output from the data generator 213 with a signal DROUT output from the memory core (101) for generating a fail indication signal ERR, indicating whether or not the memory 101 is in failure, where ERR "1" indicating a failure or ERR "0" indicating a non-failure, and where the fail address indicating portion (207) stores the address of the memory (101), when the input data and the output data are determined to be different.

And wherein the self-test circuit (BIST 105) goes into the self-test activated condition, in response to the external clock signal TCLKT and the BIST mode signal BISTON, during the BIST mode of operation.

Regarding Claims 2, 3, 4, 5, 11 and 20, Park discloses test operation mode selector circuit in the (BIST controller 211), which is part of the self-test circuit (BIST 105), and which generates a test operation command control signal CON for the memory control circuit that designates the writing or reading of the input data (DRIN) and the output data (DROUT) to / from the memory core (101),

through the write enable (WEB0 and WEB1) command. The test operation mode selector circuit generates the test operation mode signal CON by decoding a plurality of test operation mode input signals supplied from outside, such as signal TCLKT and the BIST mode signal BISTON, during the BIST mode of operation. The input signals are in synchronization with an input timing signal CLK, based on the TCLKT clock supplied from outside, FIG. 4.

Regarding Claims 6, 7, 31, 32, 36, 37 and 38, Park discloses the self-test activation signal (BISTON) supplied from the external self-test input terminal, at a prescribed potential level, such as "1" or "0", during the BIST mode of operation, as shown in FIGS. 1and 2.

Regarding Claims 8, 12 and 21, Park discloses test operation command generating circuit (BIST controller 211), which is part of the self-test circuit (BIST 105) and generates a test operation command control signal CON for the memory control circuit that designates the writing or reading, such as the write enable (WEB0 and WEB1) command corresponding to a particular test address (RADD and CADD), which is generated by the test address generating circuit (203) provided for the memory 101, where the read / write command is synchronous with the (CLK), and which is generated from the external clock signal TCLKT, see timing FIGS. 4 and 5.

Regarding Claims 9, 10, 22, 24 and 25, Park discloses a test address generating circuit (203), including an address counter 217 for generating a test address (RADD and CADD), by counting an address timing signal CLK, FIG. 4, and selectively (MUX 111) switching a non inverting output (RADD and CADD) to

the memory 101. The address-timing signal (CLK) is generated from the external clock signal TCLKT, see timing FIGS. 4 and 5.

Regarding Claims 13-15, Park discloses counter (219), where the clock counter 219 counts the number of clock cycles until an error is detected in the memory 101, and where the fail address indicating portion (207) stores the address of the memory (101), when the input data and the output data are determined to be different.

Regarding Claims 16-19 and 23, Park discloses test output circuit comparator (205) located in the BIST 105, which compares the signal output from the data generator 213 with a signal DROUT output from the memory core (101) for generating a fail indication signal ERR, indicating whether or not the memory 101 is in failure, where ERR "1" indicating a failure or ERR "0" indicating a non-failure, and where the values stored in the clock number register 221 are outputted in series, as a redundancy information extracting signal RED, synchronization with the output timing signal (external clock signal TCLKT).

Regarding Claims 27-29, and 33-35, Park discloses selector (MUX 107), which includes (MUX 109) and an (MUX 111) for switching input signals TCLKL, TCLKL, INL and BISTOUT, during the normal and the BIST mode FIG. 1 and 2, (described (column 4, line 3-32).

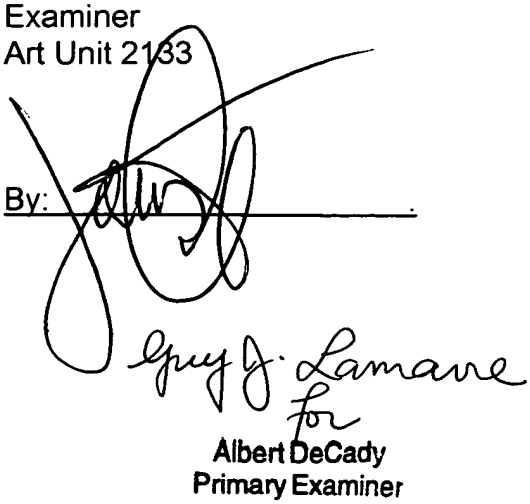
Regarding Claim 30, Park discloses data output circuit (DROUT) that outputs data from the memory 101,FIG. 2.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James C Kerveros
Examiner
Art Unit 2133

By: 

Albert DeCady
Primary Examiner

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Date: 2/9/04
Non-Final Rejection